

Abstract

A MOS semiconductor device includes n⁻-type surface regions, which are extended portions of an n⁻-type drift layer 12 extended to the surface of the semiconductor chip. Each n⁻-type surface region 14 is shaped with a stripe surrounded by a p-type well region. The surface area ratio between n⁻-type surface regions 14 and p-type well region 13 including an n⁺-type region 15 is from 0.01 to 0.2. The MOS semiconductor device further includes, in the breakdown withstand region thereof, a plurality of guard rings, the number of which is equal to or more than the number n calculated from the following equation $n = (\text{Breakdown voltage } V_{br} (\text{V})) / 100$, and the spacing between the adjacent guard rings is set at 1 ..m or less.